THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 17

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

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Ex parte MITSUYOSHI NAKAMURA

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Appeal No. 96-4081
Application 08/417,333[1]

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ON BRIEF

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Before BARRETT, FLEMING and HECKER, ***Administrative Patent Judges***.

FLEMING, ***Administrative Patent Judge***.

DECISION ON APPEAL

[1] Application for patent filed April 5, 1995.

This is a decision on appeal from the final rejection of claims 1 through 11. Claims 12 through 18 have been withdrawn from consideration.

The invention is directed to a semiconductor memory device and a manufacturing method thereof. In particular, Appellants disclose on page 1 of the specification that the invention is directed to a semiconductor memory device and manufacturing method thereof in which a single memory cell consists of a single field effect transistor.

Independent claim 1 is reproduced as follows:

1. A semiconductor memory device in which a single memory cell consists of a single field effect transistor, wherein

said field effect transistor has its source terminal connected to a source wiring having at a portion thereof a resistor with a high resistance.

The Examiner does not rely on any references for the rejection.

The specification is objected to under 35 U.S.C. § 112, first paragraph, as failing to provide an adequate written description of the invention. Claims 1 through 11

stand rejected under 35 U.S.C. § 112, first paragraph, for the reasons set forth in the objection to the specification.

Rather than reiterate the arguments of Appellant and the Examiner, reference is made to the briefs[2] and answer for the respective details thereof.

OPINION

We will not sustain the rejection of claims 1 through 11 under 35 U.S.C. § 112, first paragraph.

"The function of the description requirement [of the first paragraph of 35 U.S.C. § 112] is to ensure that the inventor had possession, as of the filing date of the application relied on, of the specific subject matter later claimed by him." ***In re Wertheim***, 541 F.2d 257, 262, 191 USPQ 90, 96 (CCPA 1976). "It is not necessary that the application describe the claim limitations exactly, . . . but only so clearly that persons of ordinary skill in the art will

[2] Appellant filed an appeal brief on August 8, 1996. Appellant filed a reply brief on August 28, 1996. The Examiner mailed a communication on September 13, 1996 which states that the reply brief has been entered and considered but no further response by the Examiner is deemed necessary.

recognize from the disclosure that appellants invented processes including those limitations." ***Wertheim***, 541 F.2d at 262, 191 USPQ at 96 ***citing In re Smythe***, 480 F.2d 1376, 1382, 178 USPQ 279, 284 (CCPA 1973). Furthermore, the Federal Circuit points out that "[i]t is not necessary that the claimed subject matter be described identically, but the disclosure originally filed must convey to those skilled in the art that applicant had invented the subject matter later claimed." ***In re Wilder***, 736 F.2d 1516, 1520, 222 USPQ 369, 372 (Fed. Cir. 1984), ***cert. denied***, 469 U.S. 1209 (1985), ***citing In re Kaslow***, 707 F.2d 1366, 1375, 217 USPQ 1089, 1096 (Fed. Cir. 1983).

The Examiner argues on page 3 of the answer that the disclosure as originally filed does not provide a description of a memory cell that consists of a single field effect transistor. On page 4 of the answer, the Examiner acknowledges that Appellant's specification on page 1, line 10, cites a single memory cell consisting of a single field effect transistor. The Examiner argues that this is reference to Figure 24 which clearly shows multiple transistors and

nowhere is it taught that the cells have only a single transistor.

Turning to Appellant's specification, we find on page 1 that Appellant discloses that the present invention relates to a semiconductor memory device in which a single memory cell
consists of a single field effect transistor. Furthermore, Appellant discloses on the same page that Figure 24 is a circuit diagram of a conventional semiconductor device having a single memory cell provided by a single enhanced type Metal Oxide Semiconductor (MOS) transistor. Furthermore, on page 2 of the specification, Appellant discloses the operation of the semi- conductor device shown in Figure 24 in which it clearly shows that each transistor operates as a single cell to record a single bit of data. On page 16 of the specification, Appellant discloses that Figure 1 is a circuit diagram of

the present invention in which the eight transistors 51-58 are enhanced type MOS transistors which each operate as a single cell of the memory.

In view of the foregoing, we reverse the decision of the Examiner rejecting claims 1 through 11 under 35 U.S.C. § 112, first paragraph.

REVERSED

LEE E. BARRETT Administrative Patent Judge	)	
MICHAEL R. FLEMING Administrative Patent Judge	)	BOARD OF PATENT APPEALS AND INTERFERENCES
STUART N. HECKER Administrative Patent Judge	)	

MRF:psb

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Application 08/417,333

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